TIS-5351 TinyClock User's Guide

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The Turn Island Systems TIS-5351 is a simple three-output squarewave clock generator with an external frequency reference input as well as an internal crystal oscillator. It is powered and configured though a USB connection.   The output frequency range is from 8 KHz to 112 MHz.

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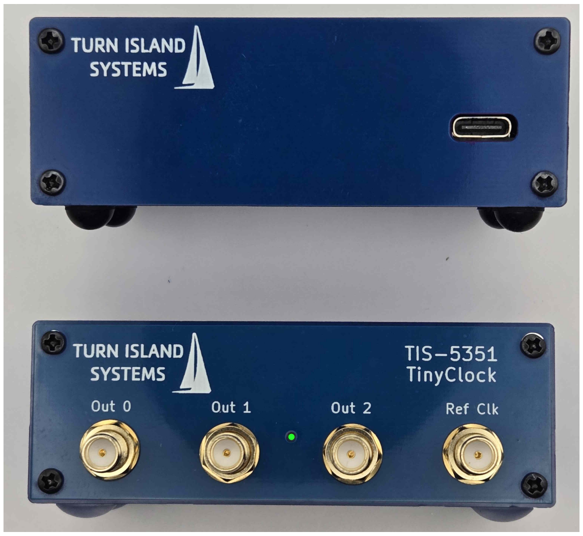
Specifications

Dimensions



Width: 3.3” / 83mm
Height: 1.3” / 33mm
Depth: 1.8” / 45mm
Weight: 2.6 oz / 74 g

Power and Control

Voltage: 5V, via USB-C connector

Current consumption:

- All outputs 1 MHz into 50 Ohm load: 0.06A
- All outputs 100 MHz into 50 Ohm load: 0.1A

Reference Clock Input

This SMA jack input accepts sine or square-wave between -10dBm and +20 dBm (between 0.1V and 6V P-P). A GPS Disciplined Oscillator is typically used. The REF CLK port provides a 50 Ohm DC termination.

Outputs

The three SMA jack outputs provide a 50 Ohm output impedance square wave, 0 / 3.3V no load, 0 / 1.6V with 50 Ohm load. The outputs can be DC or AC coupled.. The output frequency range is from 8 KHz to 112 MHz.

The Si5351A Clock Generator

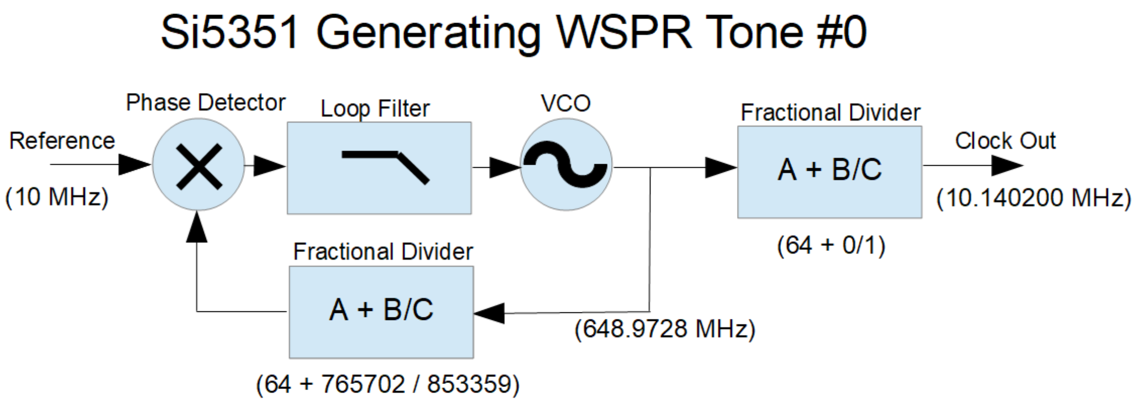


Illustration 1: Si5351 Basic Architecture

Circuit Description

Block Diagram

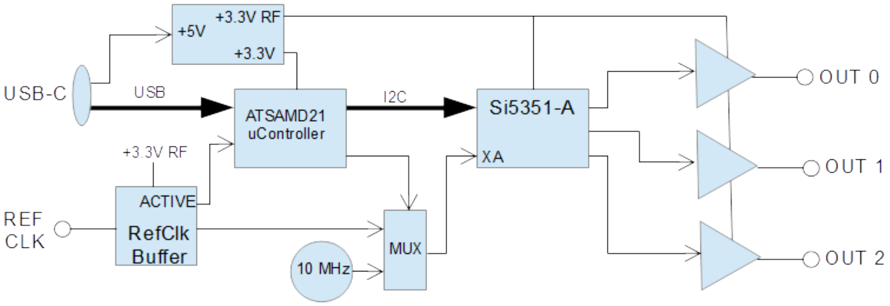


Illustration 2: TinyClock Block Diagram

Output Stage

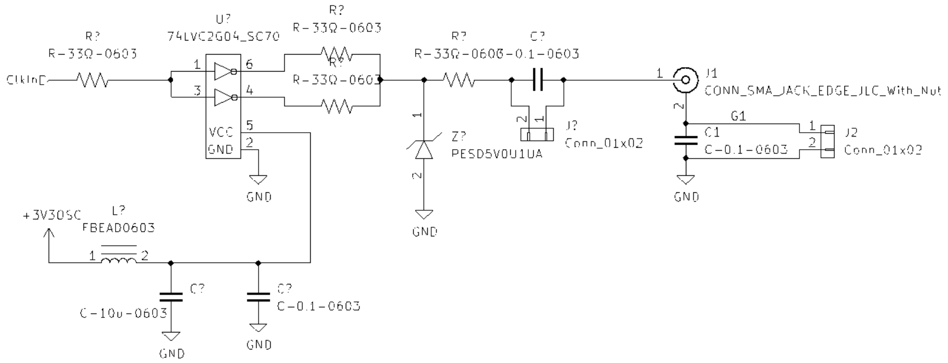


Illustration 3: TinyClock Output Stage Schematic

Each of the three output stages have a 0 to +3.3V output when unloaded. Series resistors, and the driver output impedance provide a source impedance of 50 Ohms, while a transient suppression diode provides a good degree of protection against static and other overloads.

Both the signal path and the output jack ground connection can be AC-coupled by removing the respective header-jumper (see below image).

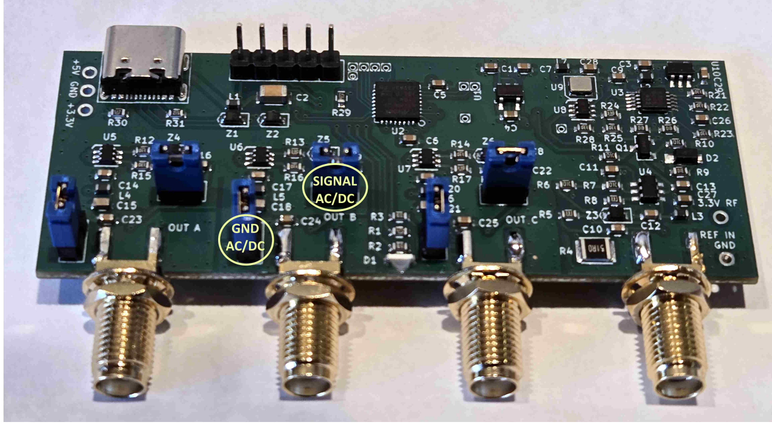


Illustration 4: TinyClock DC/AC-Coupling Jumpers

Configuration via USB Serial Port

The TinyClock is configured via the USB serial port / power connection. These settings can be saved, and will be used whenever power is applied. Once configured, no computer connection is required.

Note that when a frequency is entered it must be in Hz, or use a suffix of 'K' or 'M'. A decimal point can be used, and the suffixes can be upper or lower case ('m' means Mega, not milli)

Example: 1234567 or 1234.567K or 1.234567M

SET [channel (0/1/2)] [output freq in Hz]

This attempts to optimize all three channels for frequency accuracy and minimum spurious outputs.
First, an attempt is made to use a common PLL for all channel pairs, using integers for the PLL feedback dividers. Otherwise, channel 0 will use PLL 0, channel 1 will use PLL 1, and channel 2 will use whichever PLL provides the best solution.
The channel output dividers use even-integer divisors where possible, and fractional PLL divisors where necessary. If an even-integer solution for the channel 2 output dividers cannot be found, this divider will use fractional division.

The set frequency may not be exactly as requested, the actual frequency is shown.

ON [channel (0/1/2)] : Enable output

OFF [channel (0/1/2)] : Disable output

FREQ : Show frequencies

This shows the two PLL frequencies and the three output frequencies. These are the actual frequencies, which may vary slightly from the requested frequencies. The displayed resolution is 1 uHz, but the accuracy of this depends on the reference clock frequency.

STAT : Show Dividers and Frequencies

This shows the requested frequencies, the actual set frequencies, and the PLL and output divider values.

REF [internal / external (0/1)] [input reference frequency in Hz]

Set the internal xtal or external reference frequency. examples:
REF 0 10.000001M (set internal reference clock frequency to compensate for a measured internal oscillator frequency error)
REF 1 27M (set external reference clock frequency to 27MHz)
The reference frequency can be set to any value between 4 and 40 MHz, but the Si5351 is not guaranteed to operate beyond the 10 – 27 MHz range.

PLL [0/1] [A] [B] [C] : Set PLL Dividers

PLL feedback divider: A + B / C

example: **PLL 0 60 1 2** (set PLL0 divider to 60+1/2 -- with a 10 MHz reference this sets the PLL0 frequency to 605 MHz)

While the **SET** command will automatically calculate the appropriate PLL and Output divider values, it may be desirable to manually set these dividers using the **PLL** and **OUT** commands. Set **AUTO** off (**AUTO 0**) so these dividers will not be recalculated should the reference clock source be changed.

OUT [channel (0/1/2)], [PLL(0/1)], [A], [B], [C], [D] : Set channel pll # and output dividers

Primary output divider: A + B / C,

D is the secondary output-stage divider: 1/2/4/8/16/32/64/128

example: **OUT 1 0 20 3 100 1** (Using the PLL from the previous example, set output #1 to 605 MHz / (20 + (3/100)) / 1 = 30.204692960559... MHz)

While the **SET** command will automatically calculate the appropriate PLL and Output divider values, it may be desirable to manually set these dividers using the **PLL** and **OUT** commands. Set **AUTO** off (**AUTO 0**) so these dividers will not be recalculated should the reference clock source be changed.

INVERT [channel (0/1/2)], [1/0] : Output invert

Example: **INV 2 1** (invert the phase of channel #2)

When two channels are using the same PLL and are set to the same frequency, **INVERT** can be used in conjunction with the **PHASE** command (see below) to establish an arbitrary phase relationship between the two.

PHASE [channel (0/1/2)], [0-127] : Output phase

This sets the Si5351 channel “delay” register. For a 90 degree phase shift set phase value = output divider value. Since the maximum phase value is 127, this limits the phase-shift range of lower-frequency outputs (500 MHz PLL / 127 = 3.94... MHz).
Fractional output divider values may cause phase-shift jitter, and secondary output-stage divider values other than 1 will also “complicate” the effect of the PHASE command.

CONFIG : Show Config

Displays the current configuration parameters. The output frequencies shown are the requested frequencies (the actual output frequencies may differ)

RD : Read Config

Reads the previously-saved configuration.

SAVE : Save Config

Saves the current configuration parameters.

ECHO [1/0] : Echo on/off

Enables or disables the command-line character echo and prompt.

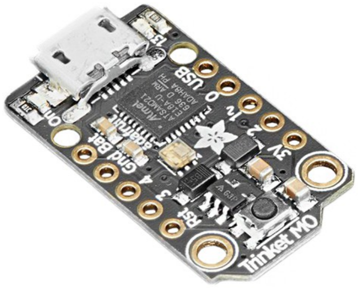
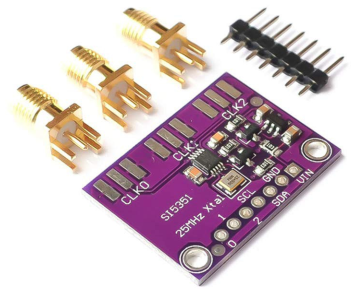
AUTO [1/0] : Enable automatic frequency set on reference change

RESET : Reset PLLs

UPDATE YES : load new program

This will halt the TinyClock for the loading of a new program
Copy the new "UF2" file into the BOOT directory, and the TinyClock will restart.

Build Your Own?

Illustration 5: Adafruit Trinket M0 	 *Illustration 6: Si5351 Breakout Board*

You can build your own simplified TinyClock using inexpensive modules available from many sources.

The Si5351 Breakout Boards contain an inexpensive and not particularly stable crystal, but this is still quite useful unless you need frequency accuracy. The Breakout Board outputs are not protected against overload or transients.

There are Arduino and other software libraries available for the Si5351, which will give you basic control to the Si5351 settings. However many of these libraries will not provide access to the more advanced features of this device.